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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,666	01/13/2001	Hiroaki Tsugane	15.29/5629	2708

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Konrad Rayness & Victor, LLP
315 South Beverly Drive, Suite 210
Beverly Hills, CA 90212

EXAMINER

SCHILLINGER, LAURA M

ART UNIT PAPER NUMBER

2813

DATE MAILED: 12/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/759,666

Applicant(s)

TSUGANE ET AL.

Examiner

Laura M Schillinger

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 September 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8, 15-23, 25 and 26 is/are pending in the application.
- 4a) Of the above claim(s) 25 and 26 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 15-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 17-19.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Amendment D, dated 9/24/03, in Paper No.20.

Election/Restrictions

Newly submitted claims 25-26 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

This application contains claims directed to the following patentably distinct species of the claimed invention:

Claim 25-26, pertains a DRAM with a third and fourth electrodes which is considered to be a separate species from originally elected claims 1-8.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 24 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-2 and 15-16, 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Koo et al ('446).

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In reference to claim 1, Koo teaches a method comprising:

- a) simultaneously forming a storage node of the capacitor and lower electrode of the capacitor (Fig.4 (16a, f, h);
- b) simultaneously forming a dielectric layer of the cell and element capacitor (Fig.4 (17a, b,c);
- c) simultaneously forming a cell plate of the capacitor and upper electrode of the capacitor element (Fig.4 (18a, b,c).

In reference to claim 2, Koo teaches further comprising: forming a word line and a connection layer between the lower electrode and a separate element (Fig.4 (16e) and Col.7, lines: 10-20).

In reference to claim 15, Koo teaches a method comprising:

- a) simultaneously forming a conductive storage node of the first capacitor and a conductive lower electrode of the second capacitor (Fig.4 (16a, f, h);
- b) simultaneously forming a dielectric layer of the first and second capacitor (Fig.4 (17a, b,c);
- c) simultaneously forming a conductive cell plate of the first capacitor and a conductive upper electrode of the second capacitor element (Fig.4 (18a, b,c).

In reference to claim 16, Koo teaches further comprising: forming a word line and a connection layer between the lower electrode and a separate element. (Fig.4 (16e) and Col.7, lines: 10-20).

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In reference to claim 20, Koo teaches further comprising performing at least one ion implantation of an impurity into part of the second conducting layer prior to the etching a portion of the second conducting layer (Col.5, lines: 35-40)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3-8, 17-19, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koo ('446) as applied to claims above, and further in view of Takada et al ('772).

In reference to claims 3-8 and 17-19, and 21-23, Koo teaches the elements of claims 1 and 15 above, however fails to teach the formation of a resistance element.

However, in reference to claim 3, Takada ('772) teaches further comprising forming a first resistance element and a second resistance element in the analog region by ion implantation (Fig.14 (resistance element) and Col.7, lines: 30-40), wherein the first element is doped more than the second (Col.8, lines: 15-30).

In reference to claim 4, Takada teaches further comprising forming a first resistance element and a second resistance element in the analog region by ion implantation (Fig.14 (resistance element)

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and Col.7 , lines: 30-40) wherein the first element is doped more than the second (Col.8, lines: 15-30).

In reference to claim 5, Takada teaches further comprising forming a first resistance element and a second resistance element in the analog region by ion implantation (Fig.14 (resistance element and Col.7 , lines: 30-40)), wherein the first element has impurity diffusion thus doping more than the second (Col.7, lines: 35-45 and Col.8, lines: 35-50).

In reference to claim 6, Takada teaches further comprising forming a first resistance element and a second resistance element in the analog region by ion implantation (Fig.14 (resistance element and Col.7 , lines: 30-40)),

Wherein the first element has impurity diffusion thus doping more than the second (Col.8, lines: 15-30).

In reference to claim 7, Takada teaches further comprising forming a first resistance element and a second resistance element in the analog region by ion implantation (Fig.14 (resistance element and Col.7 , lines: 30-40)),

Wherein the first element has a silicide layer thus less resistance than the second (Col.8, lines: 15-30).

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In reference to claim 8, Takada teaches further comprising forming a first resistance element and a second resistance element in the analog region by ion implantation (Fig.14 (resistance element and Col.7 , lines: 30-40)),

Wherein the first element has a silicide layer thus less resistance than the second (Col.8, lines: 15-30).

In reference to claim 17, Takada teaches further comprising forming a first resistance element and a second resistance element in the analog region (Fig.14 (resistance element and Col.7 , lines: 30-40)), wherein the first resistance is lower than the second (Col.8, lines: 15-30).

In reference to claim 18, Takada teaches further comprising forming a first resistance element and a second resistance element in the analog region by ion implantation (Fig.14 (resistance element and Col.7 , lines: 30-40)),

Wherein the first element is doped more than the second(Col.8, lines: 15-30).

In reference to claim 19, Takada teaches wherein the etching a portion of the second conducting layer also forms a first resistance element and a second resistance element in the analog element region (Fig.14 (resistance element and Col.7 , lines: 30-40)).

In reference to claim 21, Takada teaches wherein a number of ion implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantations of impurity in a region where the second resistance element is to be formed (Col.8,

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lines: 15-30).so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element (Fig.14 (resistance element and Col.7 , lines: 30-40)),

In reference to claim 22, Takada teaches wherein, prior to the etching a portion of the second conducting layer (Col.9, lines: 30-35), an impurity is diffused in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element (Fig.14 (resistance element and Col.7 , lines: 30-40)),

In reference to claim 23, Takada teaches wherein prior to etching a portion of the second conducting layer, a silicide layer is formed in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element (Fig.14 (resistance element and Col.7 , lines: 30-40) and (Col.9, lines: 30-35)).

It would have been obvious to one of ordinary skill in the art to modify Koo's teachings to include the resistance element formation as taught by Takada because as Takada teaches, a p-Si resistor is free of parasitic capacitance and heat which may be generated by IC devices (Col.1, lines: 25-35 and 45-50).

Response to Arguments

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Applicant's arguments with respect to claims 1-8, 15-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (703) 308-4940. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LMS

December 13, 2003



JACK CHEN
PRIMARY EXAMINER